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(71) Applicant: **Hitachi Maxell Limited**
Ibaraki-shi 567-0877 (JP)

(72) Inventors:
- **Kawamura, Satoshi**
Yokohama-shi Kanagawa 236-0021 (JP)
- **Shimizu, Shin**
Kawasaki-shi Kanagawa 214-0013 (JP)

(74) Representative: **Merryweather, Colin Henry**
J.A. Kemp & Co.
14 South Square
Gray's Inn
London WC1R 5JJ (GB)

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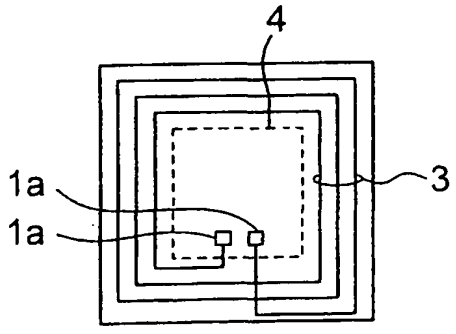
(54) Method for manufacturing an IC element including a coil

(57) A method for manufacturing an IC element in which antenna coil for wireless communication is uniformly formed, said method comprising at least steps of: terming a required conductive pattern at least including plurality of antenna coil for wireless communication over a surface protection film of a wafer formed by a predetermined process; and obtaining an IC element in which a single antenna coil is uniformly formed by way of a scriber wafer on which said required conductive pattern is formed.

FIG. 1A



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Description

[0001] The present invention relates to AN IC element formed integrally with a coil on a chip, a method of manufacturing the IC element, an information carrier incorporating the IC element and a method of manufacturing the information carrier.

[0002] Heretofore, such a contactless type information carrier has been known which includes an IC element mounted internally of a substrate having a predetermined shape and an antenna coil electrically connected to the terminals of the IC element for effectuating in a noncontacting or contactless manner reception of electric power from a reader/writer and a signal transmission/reception with the reader/writer through the medium of the electromagnetic wave. As the information carriers of this species, there may be mentioned those referred to as the card-like information carriers, the coin-like information carriers, the button-like information carriers and the like named after the external appearance.

[0003] As the information carriers of the types mentioned above, the information carrier having an antenna coil patterned on a substrate or the information carrier having an antenna coil composed of a coil carried on a substrate has heretofore been employed. However, in recent years, there has been proposed an information carrier in which the IC element formed integrally with the antenna coil is mounted on the substrate and which features the capability of being manufactured inexpensively without need for the protection processing of the interconnection points between the antenna coil and the IC element and the moisture-proof treatment and additionally the excellent durability owing to insusceptibility to breakage of coil conductor regardless of stresses induced upon bending, torsion or the like of the substrate.

[0004] As a method of forming the antenna coil on the information carrier, a sputtering method is adopted. Thus, the electric conductor of the antenna coil formed integrally with the IC element is implemented in the form of an aluminum-sputtered film.

[0005] In this conjunction, it is however noted that when the antenna coil is formed integrally on the IC element, not only the winding diameter and the conductor width of the coil become smaller when compared with the case where the antenna coil composed of the winding is carried on the substrate, but also the number of turns of the coil is naturally limited, making it difficult to increase the range or distance for communication with the reader/writer or rendering it even impossible to ensure the communication range.

[0006] In accordance with the present invention, there is provided a method for manufacturing an IC element in which antenna coil for wireless communication is uniformly formed, said method comprising the steps of:

forming a required conductive pattern at least including plurality of antenna coil for wireless communication over a surface protection film of a wafer; and

obtaining an IC element in which a single antenna coil is uniformly formed by way of scriber wafer on which said required conductive pattern is formed.

[0007] According to a second aspect, the present invention provides an IC element formed integrally with a coil, wherein a conductor constituting the above-mentioned coil is implemented in a multilayer structure including a metal-sputtered layer or alternatively a metal-evaporated layer and a metal-plated layer.

[0008] Since the metal-plated layer has an electric resistance value smaller than the metal-sputtered layer or alternatively the metal-evaporated layer, loss of the electromagnetic energy can be diminished by implementing the electric conductor of the coil in a multilayer structure composed of the metal-sputtered layer or alternatively the metal-evaporated layer and the metal-plater layer when compared with the coil conductor constituted solely by the metal-sputtered layer or alternatively the metal-evaporated layer, whereby the distance or range for communication with the reader/writer can be increased.

<IC element manufacturing method>

[0009] There is provided according to a third aspect of the present invention, an IC element manufacturing method which includes a step of forming uniformly a metal-sputtered layer or alternatively a metal-evaporated layer on a surface passivation film of a finished wafer manufactured through a predetermined process, a step of forming uniformly a photoresist layer on said metal-sputtered layer or alternatively on said metal-evaporated layer, a step of exposing said photoresist layer to light illumination in a predetermined pattern inclusive of a coil for thereby exposing said metal-sputtered layer or alternatively said metal-evaporated layer in said predetermined pattern after development, a step of laminating a metal-plated layer on exposed portions of said metal-sputtered layer or alternatively said metal-evaporated layer through an electroless plating method or alternatively an electroplating method or alternatively through a precision electroforming method, a step of eliminating the photoresist layer deposited on said finished wafer, a step of forming a predetermined conductor pattern corresponding to said predetermined pattern by etching said metal-sputtered layer or alternatively said metal-evaporated layer exposed through said metal-plated layer, and a step of obtaining a concerned IC element formed integrally with the coil by scribing said finished wafer.

[0010] According to a fourth aspect of the present invention, there is provided a method which includes a step of forming uniformly a photoresist layer on a surface passivation film of a finished wafer manufactured through a predetermined process, a step of exposing in said photoresist layer to light illumination in a predeter-

mined pattern inclusive of a coil for thereby exposing said surface passivation film in said predetermined pattern after development, a step of mounting the finished wafer undergone the development processing on a sputtering apparatus or a vacuum evaporation apparatus for forming a metal-sputtered layer or alternatively a metal-evaporated layer on exposed portion of said surface passivation film, a step of eliminating the photoresist layer deposited on said finished wafer, a step of laminating a metal-plated layer on said metal-sputtered layer or alternatively said metal-evaporated layer through an electroless plating method or alternatively through an electroplating method, and a step of obtaining a concerned IC element formed integrally with a coil by scribing said finished wafer.

[0011] As is apparent from the above, by forming the required electric conductive pattern inclusive of the coil on the finished wafer to thereby obtain the concerned IC element by scribing the finished wafer, the IC element formed integrally with the coil can be manufactured with high efficiency when compared with the case where each of the individual IC elements are formed with a coil, whereby the manufacturing cost can be reduced. Furthermore, it is possible to implement the coils of a uniform thickness with high precision for all the IC elements formed on the wafer, whereby variance or dispersion of the communication characteristics can be suppressed.

[0012] Furthermore, it is noted that when the coil is formed for each of the individual IC elements by using the sputtering method or alternatively the vacuum evaporation method and the plating method, there arises a problem concerning the insulation quality of the IC element due to deposition of unnecessary conductors on an outer peripheral portion of the IC element. Of course, when the required electric conductive pattern inclusive of the coil is formed on the finished wafer, the unnecessary conductors may be deposited on the out peripheral portion of the finished wafer upon sputtering or the like process. However, the outer peripheral portion mentioned just above is intrinsically to be disposed of as the unnecessary portion. Accordingly, there will arise no problem in respect to the insulation quality of the individual IC elements.

<IC>

[0013] According to a further aspect, the present invention provides an information carrier including a substrate having mounted thereon an IC element formed integrally with an antenna coil, wherein said IC element is disposed at a center portion of said substrate in a planar direction perpendicular to a plane of said substrate.

[0014] By disposing the IC element on the substrate at the center portion as viewed in the planar direction of the substrate as mentioned above, the center of the coil formed integrally with the IC element and that of the antenna coil for the reader/writer can be easily aligned to each other. Thus, the coefficient of the electromagnetic coupling between both coils can be increased, whereby the electric power supply to the information carrier from the reader/writer as well as the signal transmission/reception between the reader/writer and the information carrier can be carried out with enhanced reliability. In particular, when the substrate which constitutes the information carrier is shaped in a square shape, a regular-polygonal shape or the like which exhibits no or less directivity relative to the reader/writer, the center of the coil formed integrally on the IC element can be aligned more easily with that of the antenna coil provided for the reader/writer, which allows the information carrier to be handled more facilitatively.

[0015] Advantageously, the IC manufacturing method provided according to a third aspect of the present invention includes a step of bonding together a first strip material having regularly formed therein a number of through-holes in which IC elements can be inserted, respectively, and a second strip material formed with no through-hole, a step of placing and fixing the IC elements each formed integrally with a coil in said through-holes, respectively, a step of bonding together said first strip material and aa third strip material having no through-hole, and a step of punching said first to third integrally bonded strip materials to thereby obtain the concerned information carriers each incorporating said IC element.

[0016] Advantageously, the IC manufacturing method provided according to a fourth aspect of the present invention includes a step of placing and fixing coils formed discretely independent of IC elements, respectively, in a number of ring-like recesses formed in a first strip material concentrically around through-holes, which are formed regularly in said first strip material and in which said IC elements can be inserted, respectively, a step of bonding a second strip material having no through-hole onto one surface of said first strip material, a step of placing fixedly said IC elements each formed integrally with a coil in said through-holes, respectively, a step of bonding together said first strip material and a third strip material having no through-hole, and a step of punching said first to third strip materials bonded integrally, to thereby obtain desired information carriers each including the IC element and the coil formed discretely independent of said IC element.

[0017] As is apparent from the above, the strip lamination in which the required IC elements (or alternatively the IC elements and the coils) are embedded is manufactured, whereon the concerned or desired information carriers are formed by punching the strip lamination. Thus, the identical information carriers can be manufactured with high efficiency, whereby the cost involved in manufacturing the desired information carriers can be reduced.

[0018] Incidentally, in the manufacturing methods according to the third and fourth aspects described above, the substrate of the information carrier is formed of three members (i.e., the first to third strip members), it is

equally possible to implement the substrate for the information carrier with two members by forming the recesses for accommodating the IC elements, respectively, in the first strip material instead of adopting the structure in which the through-holes for accommodating the IC elements, respectively, are formed in the first strip material.

[0019] Furthermore, in the manufacturing methods according to the third and fourth aspects described above, the IC elements (or the IC elements and the coils) are completely embedded internally of the strip materials. However, it is also possible to make the IC elements (or the IC elements and the coils) be exposed exteriorly from one surface of the strip material by sealing off the through-holes or
the recesses formed in the strip material with a resin after having placed the IC elements (or the IC elements and the coils) in the through-holes or the recesses, respectively.

[0020] Besides, when the IC elements (or the IC elements and the coils) is to be exposed externally of the one surface of the strip material, the substrate of the information carrier can be formed by a single member by forming the recesses for accommodating the respective IC elements (or the IC elements and the coils) in the strip material.

[0021] Embodiments of the present invention will now be described by way of non-limitative example with reference to the accompanying drawings, in which:

Figures 1A, 1B and 1C are plan views showing IC elements according to exemplary embodiments, respectively.
Figures 2A and 2B are sectional views showing major portions of IC elements according to exemplary embodiments, respectively.
Figure 3 is a plan view showing a finished wafer.
Figures 4A, 4B, 4C, 4D, 4E and 4F are views for illustrating stepwise a first example of an IC element manufacturing method according to the present invention.
Figures 5A, 5B, 5C, 5D and 5E are views for illustrating stepwise a second example of the IC element manufacturing method according to the present invention.
Figure 6 is a plan view showing a finished wafer having formed thereon a required electric conductive pattern inclusive of an antenna coil.
Figure 7 is a partially broken plan view of an information carrier according to a first exemplary embodiment.
Figure 8 is a developed perspective view showing the information carrier according to the first exemplary embodiment.
Figure 9 is a sectional view of the information carrier according to the first exemplary embodiment.
Figure 10 is a view illustrating the information carrier according to the first exemplary embodiment in the state being used.
Figure 11 is a sectional view of an information carrier according to a second exemplary embodiment.
Figure 12 is a sectional view of an information carrier according to a third exemplary embodiment.
Figure 13 is a sectional view of an information carrier according to a fourth exemplary embodiment.
Figure 14 is a sectional view of an information carrier according to a fifth exemplary embodiment.
Figure 15 is a sectional view of an information carrier according to a sixth exemplary embodiment.
Figure 16 is a sectional view of an information carrier according to a seventh exemplary embodiment.
Figure 17 is a sectional view of an information carrier according to an eighth exemplary embodiment.
Fig. 18 is a fragmental perspective view showing a first example of a strip material.
Fig. 19 is a fragmental perspective view showing a second example of the strip material.
Fig. 20 is a fragmental perspective view showing a third example of the strip material.
Fig. 21 is a fragmental perspective view showing a fourth example of the strip material.
Fig. 22 is a fragmental perspective view showing a fifth example of the strip material.

<IC element>

[0022] In the following, description will be made of IC elements according to exemplary embodiments of the present invention by reference to Figs. 1A, 1B and 1C together with Figs. 2A and 2B, wherein Figs. 1A, 1B and 1C are plan views showing the IC elements according to the exemplary embodiments, respectively, of the invention and Figs. 2A and 2B are sectional views showing major portions of the IC elements according to the exemplary embodiments, respectively, of the invention.

[0023] As is shown in Figs. 1A, 1B and 1C and Figs. 2A and 2B, in each of the IC elements according to the instant exemplary embodiments, an antenna coil 3 of a rectangular spiral pattern is formed integrally on a surface of the IC element 1 in which input/output terminals 1a thereof are formed through the medium of an electrically insulative surface passivation film 2 such as a silicon oxide film, a resin film or the like.

[0024] In the case of the IC element 1 shown in Fig. 1A, the antenna coil 3 is formed only in an outer peripheral portion exclusive of a circuit forming portion 4. By virtue of this structure, appearance of stray capacitance between the circuit formed in the IC element 1 and the antenna coil 3 can be prevented, whereby the efficiency of electric power reception from a reader/writer as well as the efficiency of signal transmission/reception with the reader/writer can be enhanced.

[0025] In the case of the IC element 1 shown in Fig. 1B, the antenna coil 3 is so formed as to extend over the circuit forming portion 4. With this structure, the number of turns of the antenna coil can be increased,

whereby the efficiency of power reception from the reader/writer as well as the efficiency of signal transmission/reception with the reader/writer can be much enhanced.

[0026] Incidentally, in the case of the exemplary embodiment shown in Fig. 1B, the antenna coil is overlaid partially on the circuit forming portion 4. However, it is equally possible to form the antenna coil over the whole circuit forming portion 4 with a view to implementing the IC element in a miniature size at low cost.

[0027] In the IC element 1 shown in Fig. 1C, corner portions of the antenna coil 3 formed in a rectangular spiral pattern are chamfered obliquely. Owing to this feature, current concentration in the corner portions can be prevented with the resistance value of the antenna coil 3 being thereby decreased, as a result of which the efficiency of power reception from the reader/writer as well as the efficiency of signal transmission/reception with the reader/writer can be much more enhanced. The corner portion may be chamfered arcuately substantially to the same effect. Furthermore, although it is preferred to chamfer both the inner and outer peripheral edge portions of the individual turns, only the outer peripheral edge portions may be chamfered substantially to the _similar effect.

[0028] In any cases of the antenna coils 3 described above, the line width of the antenna coil 3 should preferably be greater than 7 μm inclusive, the interturn distance should preferably be shorter than 5 μm inclusive and the number of turns should preferably be greater than 20 turns inclusive in order to ensure that sufficient electric power can be fed to the antenna coil while realizing desirable characteristics for the communication with the reader/writer in practical applications.

[0029] Interconnection of the input/output terminals 1a of the IC element 1 and the antenna coil 3 are made through-holes 5 opened in the surface passivation film 2. In that case, the diameter or width of the through-hole 5 should preferably be sized smaller than the line width of the antenna coil 3, as can be seen in Figs. 2A and 2B, so that the input/output terminal 1a and the antenna coil 3 can be interconnected without fail even in the case the position at which the antenna coil 3 is formed deviated more or less from that of the antenna coil.

[0030] The conductor constituting the antenna coil 3 is implemented in a multilayer structure which includes a metal-sputtered layer or alternatively a metal-evaporated layer 6 and a metal-plated layer 7, as shown in Figs. 2A and 2B. In the case of the example shown in Fig. 2A, the metal-plated layer 7 is formed only on the top surface of the metal-sputtered layer or alternatively metal-evaporated layer 6. On the other hand, in the case of the example shown in Fig. 2B, the metal-plated layer 7 is so formed as to cover the whole surface of the metal-sputtered layer or alternatively metal-evaporated layer 6. The metal-sputtered layer or alternatively metal-evaporated layer 6 and the metal-plated layer 7 can be formed of a given electrically conductive metal or metals. However, it is preferred to form the metal-sputtered layer or alternatively metal-evaporated layer 6 of aluminum or nickel or copper or chromium because of relatively low cost and high electric conductivity. Further, the antenna coil can be formed in a single layer or in a laminated structure including a combination of plural layers, as can be seen in Figs. 2A and 2B. The metal-plated layer 7 should preferably be formed of copper by resorting to a non-electrolytic plating method or an electroplating method or a precision electroforming method.

<IC element manufacturing method>

[0031] Next, description will be made of exemplary embodiments of the IC element manufacturing method according to the present invention by reference to Figs. 3 to Fig. 6, wherein Fig. 3 is a plan view of a so-called finished wafer which has been completed through predetermined treatment processes, Figs. 4A, 4B, 4C, 4D, 4E and 4F are views for illustrating stepwise a first example of the IC element manufacturing method according to the present invention, Figs. 5A, 5B, 5C, 5D and 5E are views for illustrating stepwise a second example of the IC element manufacturing method according to the present invention, and Fig. 6 is a plan view of a finished wafer having formed thereon a required conductive pattern inclusive of the antenna coil.

[0032] As is shown in Fig. 3, a large number of circuits 12 for the IC element are formed with equidistance in an inner portion exclusive of the outermost peripheral portion, wherein the surface passivation film 2 is formed over the surface on which the circuits for the IC element are formed (see Figs. 4 and 5).

[0033] In the IC element manufacturing method according to a first exemplary embodiment shown in Figs. 4A, 4B, 4C, 4D, 4E and 4F, the metal-sputtered layer or alternatively metal-evaporated layer 6 is formed uniformly on the surface passivation film 2 deposited on the circuit-formed surface of the finished wafer 11 by using aluminum or an aluminum alloy or alternatively copper or a copper alloy, as is shown in Fig. 4A. Subsequently, a photoresist layer 12 is uniformly formed on the metal-sputtered layer or alternatively metal-evaporated layer 6 and then the photoresist layer as formed is covered with a mask 13 of a required pattern inclusive of the coils, whereon the photoresist layer 12 is exposed to illumination of light rays 14 of a predetermined wavelength externally of the mask 13, as is shown in Fig. 4B. Thereafter, the photoresist layer 12 undergone the light exposure is subjected to a developing process, whereby the light-exposed portions of the photoresist layer 12 are removed, as a result of which the portions of the metal-sputtered layer or alternatively metal-evaporated layer 6 which correspond to the above-mentioned light exposure pattern is exposed outwardly, as is shown in Fig. 4C. The exposure pattern of the metal-sputtered layer or alternatively metal-evaporated layer 6 includes a ring-shaped electrode portion 15, the antenna coils 3 formed on the portions opposite to the aforementioned circuits

12, respectively, and lead portions 16 for connecting the individual antenna coils 3 and the electrode portion 15, as is shown in Fig. 6. In succession, by making use of the above-mentioned electrode portion 15 as one electrode, electroplating or precision electroforming process is performed on the exposed portions of the metal-sputtered layer or alternatively metal-evaporated layer 6, to thereby laminate the metal-plated layers 7 on the exposed portions of the metal-sputtered layer or alternatively metal-evaporated layer 6, as is shown in Fig. 4D. Subsequently, the photoresist layer 12 deposited on the surface of the finished wafer 11 is removed through an ashing or the like process to thereby obtain the finished wafer 11 formed with the metal-plated layer 7 including the electrode portion 15, the antenna coils 3 and the lead portions 16 deposited on the uniform metal-sputtered layer or alternatively metal-evaporated layer 6, as shown in Fig. 4E. In succession, the metal-sputtered layer or alternatively metal-evaporated layer 6 exposed through the metal-plated layer 7 is selectively etched to thereby remove the metal-sputtered layer or alternatively metal-evaporated layer 6 exposed externally through the metal-plated layer 7, as is shown in Fig. 4F. Thus, there is obtained the finished wafer 11 on which both the metal-sputtered layer or alternatively metal-evaporated layer 6 and the metal-plated layer 7 are formed in the required conductive pattern shown in Fig. 6. Finally, the finished wafer 11 mentioned just above is scribed to obtain the desired IC elements 1 shown in Fig. 1.

[0034] Incidentally, in the exemplary embodiment described above, the electroplating method or precision electroforming method is adopted as the process for forming the metal-plated layer 7. It should however be understood that instead of these methods, an electroless plating method may be resorted to for forming the metal-plated layer 7 mentioned above. In that case, since no electrode is required for forming the metal-plated layer 7, it is unnecessary to form the electrode portion 15 and the lead portions 16 upon exposure of the photoresist layer 12 to light illumination.

[0035] The electroless plating method is also referred to as the chemical plating and destined for deposition of metal ions by immersing a substrate metal in a bath containing a metallic salt solution of plating metal. The electroless plating method features that a metal-plated layer which exhibits high adhesion and having a uniform and adequate thickness can be formed with relatively simple equipment. The metallic salt mentioned above serves as a supply source of metal ions to be deposited. For plating with copper, a solution of copper sulfate, cupric chloride, copper nitrate or the like is used as the plating solution. The metal ions such as copper ions or the like ions are deposited only on the metal-sputtered layer or alternatively metal-evaporated layer 6 serving as the substrate and not deposited on the electrically insulative surface passivation film 2 (or passivation film). The substrate is required to exhibit less ionization tendency for the plating metal ions and exhibit a catalytic action for deposition of the plating metal ions. Such being the circumstances, when the metal-sputtered layer or alternatively metal-evaporated layer 6 formed of aluminum is to be plated with copper, it is preferred to carry out a pretreatment of forming a nickel film of several m or less in thickness on the surface of the aluminum layer for substituting nickel for zinc by immersing in a zinc nitrate solution for several seconds.

[0036] On the other hand, in the electroplating method and the precision electroforming method, the finished wafer 11 having the metal-sputtered layer or alternatively metal-evaporated layer 6 formed thereon and an electrode made of a plating metal are immersed in a plating bath containing plating metal ions, whereon a voltage is applied across the metal-sputtered layer or alternatively metal-evaporated layer 6 formed on the finished wafer 11 and serving as the cathode and the electrode immersed in the plating bath and serving as the anode, to thereby deposit the metal ions contained in the plating bath on the surface of the metal-sputtered layer or alternatively metal-evaporated layer 6. In the electroplating method or the precision electroforming method, a solution of copper sulfate, cupric chloride, copper nitrate or the like is employed as the plating solution for plating with copper.

[0037] The IC element manufacturing method according to the instant exemplary embodiment is so arranged that the required conductive pattern inclusive of coils is first formed on the finished wafer 11, whereon the finished wafer 11 is scribed to thereby obtain the desired IC element 1. Thus, the IC elements each formed integrally with the coil can be manufactured with high efficiency at lower manufacturing cost when compared with the case where the individual coils are each formed on the individual IC elements, respectively. Besides, it is possible to form the coils in a uniform thickness, respectively, for all the IC elements formed on the wafer with high precision, as a result of which dispersion or variance of the communication characteristics can be diminished. Furthermore, if the coil is formed for each of the individual IC elements by using the sputtering method or alternatively the vacuum evaporation method and the plating method, unwanted electrical conductor materials will be deposited on the outer peripheral portion of the IC element, giving rise to a problem in respect to the insulation quality of the IC element. Similarly, in the case the required conductive pattern inclusive of the coil is formed on the finished wafer 11, unwanted conductive materials may be deposited on the outer peripheral portion of the finished wafer 11 upon sputtering or the like process. However, since the outer peripheral portion mentioned above is intrinsically destined to be disposed of as the unwanted portion, adverse influence to the insulation quality of the individual IC elements can be avoided. Additionally, in the IC element manufacturing method according to the instant example, the metal-plated layer 7 is formed in the state where the photoresist layer 12 has been deposited, and thereafter the por-

tions of the metal-sputtered layer or alternatively metal-evaporated layer 6 where the metal-plated layer 7 is not laminated are removed by etching. Thus, the metal-plated layer 7 is laminated only on the top surface of the metal-sputtered layer or alternatively metal-evaporated layer 6 without spreading widthwise. Owing to these features, the antenna coil 3 can be formed with high accuracy or precision, which in turn means that the antenna coil 3 having an increased number of turns can be formed within a narrow space.

[0038] On the other hand, in the case of the IC element manufacturing method according to a second exemplary embodiment shown in Fig. 5, a photoresist layer 12 is uniformly formed over the surface passivation film 2 formed on the finished wafer 11 and then the photoresist layer 12 as formed is covered with a mask 13 of a required pattern inclusive of coils, whereon the photoresist layer 12 is exposed to illumination of light rays 14 of a predetermined wavelength externally of the mask 13, as is shown in Fig. 5A. Thereafter, the photoresist layer 12 exposed undergoes a developing process, whereby the light-exposed portions of the photoresist layer 12 are removed so that the portions of the surface passivation film 2 which correspond to the above-mentioned light exposure pattern are exposed externally as is shown in Fig. 5B. The light exposure pattern for the photoresist layer 12 can be so formed as to include an electrode portion 15, antenna coils 3 and lead portions 16, as is shown in Fig. 6. Subsequently, the finished wafer 11 undergone the developing process is mounted on a sputtering apparatus or a vacuum evaporation apparatus and then the metal-sputtered layer or alternatively metal-evaporated layer 6 is formed on the exposed portions of the surface passivation film 2 mentioned above, as is shown in Fig. 5C. In succession, the photoresist layer 12 remaining deposited on the finished wafer 11 is removed through the ashing or like process, as is shown in Fig. 5D. Thereafter, by employing the above-mentioned electrode portion 15 as one electrode, electroplating is performed on the metal-sputtered layer or alternatively metal-evaporated layer 6, to thereby laminate the metal-plated layer 7 on the exposed portions of the metal-sputtered layer or alternatively metal-evaporated layer 6, as is shown in Fig. 5E. Finally, the finished wafer 11 mentioned above is scribed for thereby obtaining the desired IC element 1 shown in Fig. 1.

[0039] Incidentally, in the exemplary embodiments described above, the electroplating method is adopted as the means for forming the metal-plated layer 7. It should however be understood that instead of such method, an electroless plating method may be adopted for forming the metal-plated layer 7 mentioned above. In that case, since no electrode is required for forming the metal-plated layer 7, it is unnecessary to form the electrode portion 15 and the lead portions 16 upon exposure of the photoresist layer 12 to the light rays.

[0040] The IC element manufacturing method according to the instant example can assure the similar advantageous effects as those of the IC element manufacturing method according to the first exemplary embodiment and additionally allows the number of the steps of forming the conductor pattern on the finished wafer 11 to be decreased, whereby the IC element formed integrally with the antenna coil can be manufactured at higher efficiency.

<Information carrier>

[0041] In the following, description will be made of information carriers according to exemplary embodiments of the present invention by reference to Figs. 7 to 17. Figure 7 is a plan view of an information carrier according to a first exemplary embodiment with a portion being broken away, Fig. 8 is a developed perspective view showing the information carrier according to the first exemplary embodiment, Fig. 9 is a sectional view of the information carrier according to the first exemplary embodiment, Fig. 10 is a view showing the information carrier according to the first exemplary embodiment in the state being used, Fig. 11 is a sectional view of an information carrier according to a second exemplary embodiment, Fig. 12 is a sectional view of an information carrier according to a third exemplary embodiment, Fig. 13 is a sectional view of an information carrier according to a fourth exemplary embodiment, Fig. 14 is a sectional view of an information carrier according to a fifth exemplary embodiment, Fig. 15 is a sectional view of an information carrier according to a sixth exemplary embodiment, Fig. 16 is a sectional view of an information carrier according to a seventh exemplary embodiment, and Fig. 17 is a sectional view of an information carrier according to an eighth exemplary embodiment.

[0042] An information carrier 20a according to the first exemplary embodiment is comprised of a coin-like substrate 21 formed circularly in the planar shape and an IC element 1 mounted on the substrate 21 at a center portion as viewed planewise and thicknesswise of the substrate, as is shown in Figs. 7 to 9. As the IC element 1, the IC element which is formed integrally with the antenna coil, as shown in Fig. 1 and Fig. 2, is employed.

[0043] The substrate 21 is composed of a top member 22, an intermediate member 23 and a bottom member 24 which are integrally bonded together through interposed adhesive layers 25, respectively, as is shown in Fig. 8 and Fig. 9. Each of individual members 22, 23 and 24 constituting the substrate 21 may be formed of a paper sheet or a plastics sheet. However, it is preferred above all to form these members of paper sheets, respectively, in consideration of their susceptibility to the spontaneous decomposition after having been scrapped, less generation of harmful gases in incineration and inexpensiveness. Of course, it is possible to form one or two of the members 22, 23 and 24 of a paper sheet with the other one or two members being formed of a plastics sheet.

[0044] Formed in the intermediate member 23 at a

center portion thereof is a through-hole 27 into which the IC element 1 can be inserted. Thus, by bonding together the members 22, 23 and 24, a chamber in which the IC element 1 can be accommodated is formed. Incidentally, the IC element 1 should preferably be bonded fixedly to the bottom member 24 with a view to protecting the IC element from quaking upon handling of the information carrier. In that case, it is preferred from the standpoint of the manufacturing cost to form uniformly the adhesive layer 25 over one surface of the bottom member 24 so that bonding of the intermediate member 23 and the bottom member 24 on one hand and the bonding of the bottom member 24 and the IC element 1 on the other hand can be realized by making use of the adhesive layer 25. Further, the planar shape of the through-hole 27 may be selected arbitrarily. However, it is preferred from the manufacturing viewpoint to form the through-hole 27 in a circular shape, as shown in Fig. 7 and Fig. 8, because in that case there arises no necessity for precise alignment of orientation of the IC element 1 in the rotational direction with a recess which is formed by bonding together the intermediate member 23 and the bottom member 24, when the IC element is placed in that recess.

[0045] By virtue of such arrangement that the IC element 1 is disposed at a center portion of the substrate 21 formed in a circular form as viewed in the planar direction, i.e., perpendicularly to the plane of the substrate, in the case of the information carrier 20a according to the instant exemplary embodiment, the information carrier 20 can be placed within a slot 101 formed substantially semicircularly in a reader/writer 100 equipped with an antenna coil 102 for contactless communication and disposed at a center of an arcuate portion of the slot 101. In that case, the antenna coil 3 formed integrally with the IC element 1 can automatically be centered or aligned with the antenna coil 102 of the reader/writer 100, as can be seen in Fig. 10, whereby the electromagnetic coupling between both the coils 3 and 102 can be increased, as a result of which electric power supply to the information carrier 20 from the reader/writer 100 as well as signal transmission/reception between the reader/writer 100 and the information carrier 20 can be carried out with high reliability. Furthermore, because the information carrier 20a is shaped in a circular form as viewed in the planar direction, i.e., perpendicularly to the plane of the information carrier, the information carrier exhibits no directivity relative to the slot 101 formed substantially semicircularly, whereby excellent handleability of the information carrier can be ensured. Besides, because the IC element 1 is completely embedded within the substrate 21, not only high protection effectivity and excellent durability but also good aesthetic appearance owing to invisibility of the IC element 1 can be ensured for the information carrier.

[0046] Referring to Fig. 11, an information carrier 20b according to the second embodiment includes a substrate 21 constituted by a top member 22, an intermediate member 23 and a bottom member 24 and features disposition of a booster coil 28 in a concentric circular array around the IC element 1. In the figure, reference numeral 29 denotes a recess for accommodating therein the booster coil 28, wherein the recess is formed in a ring-like shape around a through-hole 27 of the intermediate member 23. In the other respects, the structure of the information carrier according to the second exemplary embodiment is identical with that of the information carrier 20a according to the first exemplary embodiment. Accordingly, repeated description thereof is omitted. The information carrier 20b according to the instant exemplary embodiment presents similar advantageous effects as those of the information carrier 20a according to the first exemplary embodiment. In addition, by virtue of the concentric circular disposition of the booster coil 28 aground the IC element 1, the electromagnetic coupling between the antenna coil 3 formed integrally with the IC element 1 and the antenna coil 102 of the reader/writer 100 can be increased owing to interposition of the booster coil 28, whereby stabilization of the electric power as well as stabilization of the signal transmission/reception can further be enhanced with the communication range being also increased.

[0047] Referring to Fig. 12, an information carrier 20c according to the third exemplary embodiment includes a substrate 21 which is constituted by two members, i.e., a top member 22 and a bottom member 24, and features a recess 30 formed in the bottom member 24 for accommodating therein the IC element 1. In the other respects, the structure of the information carrier 20c according to the third exemplary embodiment is identical with that of the information carrier 20a according to the first exemplary embodiment. Accordingly, repeated description thereof is omitted. The information carrier 20c according to the instant exemplary embodiment presents similar advantageous effects as those of the information carrier 20a according to the first exemplary embodiment. Besides, because the number of the parts constituting the information carrier is small, more inexpensive implementation of the information carrier can be realized.

[0048] Referring to Fig. 13, the information carrier 20d according to the fourth exemplary embodiment includes a substrate 21 which is constituted by two members, i.e., a top member 22 and a bottom member 24, and features a first recess 30 formed in the bottom member 24 for accommodating therein the IC element 1 and a second recess 29 formed for accommodating therein a booster coil 28. In the other respects, the structure of the information carrier 20d according to the third exemplary embodiment is identical with that of the information carrier 20c according to the third exemplary embodiment. Accordingly, repeated description thereof is omitted. The information carrier 20c according to the instant exemplary embodiment presents similar advantageous effects as those of the information carrier 20b according to the second exemplary embodiment. Besides, be-

cause the number of the parts constituting the information carrier is small, more inexpensive implementation of the information carrier can be realized.

[0049] Referring to Fig. 14, the information carrier 20e according to the fifth exemplary embodiment includes a substrate 21 which is constituted by two members, i.e., a top member 22 in which a through-hole 27 for accommodating therein the IC element and a bottom member 24 in which no through-hole 27 is formed, and features that the IC element 1 is accommodated within a recess formed by bonding together the top member 22 and the bottom member 24 with the interior of the recess being sealed off by filling a potting resin 31. In the other respects, the structure of the information carrier 20e according to the fifth exemplary embodiment is identical with that of the information carrier 20a according to the first exemplary embodiment. Accordingly, repeated description thereof is omitted. The information carrier 20e according to the instant exemplary embodiment exhibits similar advantageous effects as those of the information carrier 20a according to the first exemplary embodiment except that the IC element 1 is not covered with the substrate.

[0050] Referring to Fig. 15, the information carrier 20f according to the sixth exemplary embodiment features a substrate 21 constituted by two members, i.e., a top member 22 in which a through-hole 27 for accommodating therein the IC element and a recess 29 for accommodating a booster coil are concentrically formed around a through-hole 27 and a bottom member 24 which has neither the through-hole 27 nor the recess 29, wherein the booster coil 28 is placed within the recess 29 with the recess 29 being sealed off with a potting resin 31 while the IC element 1 is accommodated within a recess formed by bonding together the top member 22 and the bottom member 24 with that recess also being sealed off with the potting resin 31. In the other respects, the structure of the information carrier 20f according to the sixth exemplary embodiment is identical with that of the information carrier 20e according to the fifth exemplary embodiment. Accordingly, repeated description thereof is omitted. The information carrier 20f according to the instant exemplary embodiment exhibits similar advantageous effects as those of the information carrier 20a according to the first exemplary embodiment except that the IC element 1 is not covered with the substrate.

[0051] Referring to Fig. 16, the information carrier 20g according to the seventh exemplary embodiment features a substrate 21 constituted by a single member having one surface formed with a recess 30 for accommodating the IC element 1, which recess is sealed off with a potting resin 31 after the IC element 1 has been disposed therein. In the other respects, the structure of the information carrier 20g according to the seventh exemplary embodiment is identical with that of the information carrier 20e according to the fifth exemplary embodiment. Accordingly, repeated description thereof is omitted. The information carrier 20g according to the instant exemplary embodiment presents similar advantageous effects as those of the information carrier 20e according to the fifth exemplary embodiment. Besides, because the number of the parts constituting the information carrier is small, more inexpensive implementation of the information carrier can be realized.

[0052] Referring to Fig. 17, the information carrier 20h according to the eighth exemplary embodiment features a substrate 21 constituted by a single member which has one surface formed with a first recess 30 for accommodating therein the IC element 1 and a second recess 29 for accommodating therein a booster coil 28, wherein the IC element 1 is disposed within the first recess 30 mentioned above with this recess being sealed off with a potting resin 31 while the booster coil 28 is accommodated within the second recess 29 mentioned above with this recess being also sealed off with the potting resin 31. In the other respects, the structure of the information carrier 20h according to the eighth exemplary embodiment is identical with that of the information carrier 20g according to the seventh exemplary embodiment. Accordingly, repeated description thereof is omitted. The information carrier 20h according to the instant exemplary embodiment presents similar advantageous effects as those of the information carrier 20f according to the sixth exemplary embodiment. Besides, because the number of the parts constituting the information carrier is small, more inexpensive implementation of the information carrier can be realized.

[0053] At this juncture, it is to be mentioned that in the exemplary embodiments described above, the substrate 21 is formed circularly as viewed in the planar direction, i.e., perpendicularly to the plane of the substrate. It should however be appreciated that the substrate may be formed in other appropriate shapes such as square, rectangle, triangle or polygon, etc..

[0054] Further, in the case of the information carriers according to the second, fourth sixth and eighth exemplary embodiments, the discrete booster coil 28 is disposed in the through-hole and the recess formed in the substrate 21. It should however be understood that the booster coil 28 can directly be formed on the member constituting the substrate 21 by printing, plating, sputtering or the like process.

[0055] Furthermore, by implementing the booster coil 28 with a first coil for performing contactless communication with the IC element and a second coil of a greater capacity than the first coil for performing communication with an external reader/writer with and interconnecting the first and second coils in series to each other, the communication range or coverage can be extended.

<Method of manufacturing the information carrier>

[0056] Next, exemplary embodiments of the information carrier manufacturing method according to the present invention will be described by reference to Fig.

18 to Fig. 22. Figure 18 is a fragmental perspective view showing a first example of a strip material employed in manufacturing an information carrier according to the present invention, Fig. 19 is a fragmental perspective view showing a second example of the strip material, Fig. 20 is a fragmental perspective view showing a third example of the strip material, Fig. 21 is a fragmental perspective view showing a fourth example of the strip material, and Fig. 22 is a fragmental perspective view showing a fifth example of the strip material.

[0057] In the information carrier manufacturing method according to the present invention, required parts to be mounted inclusive of the IC element 1 are disposed fixedly on a raw material (strip material) for implementing a unitary substrate formed in a strip-like shape, whereon other strip material or materials is bonded onto one or both surfaces of the strip material, as the case may be, or alternatively potting for the parts to be mounted are carried out, and thereafter the concerned information carriers are punched by die-cutting from the single or the unitary bonded strip. For carrying out the information carrier manufacturing method according to the present invention, there may be selectively employed a strip material 41 in which through-holes 27 for accommodating the IC elements 1, respectively, are formed with a constant interspace, as shown in Fig. 18, a strip material 42 in which through-holes 27 are formed with a constant interspace for accommodating the IC elements 1, respectively, and in which ring-shaped recesses 29 destined for accommodating booster coils 28, respectively, are formed concentrically around the through-holes 27 with adhesive layers 32 being applied onto bottom surfaces of the ring-shaped recesses 29, respectively, as shown in Fig. 19, a strip material 43 in which recesses 30 are formed with a constant interspace for accommodating therein the IC elements 1, respectively, with an adhesive layer 32 being applied onto a bottom surface of each of the recesses 30, as shown in Fig. 20, a strip material 44 in which first recesses 30 are formed with a constant interspace for accommodating therein the IC elements 1, respectively, and in which second recesses 29 each of a ring-like shape are concentrically formed around the first recesses 30, respectively, with adhesive layers 32 being applied onto the bottom surfaces of the recesses 29 and 30, respectively, as shown in Fig. 21, or a strip material 45 on which neither through-holes nor recesses are formed but an adhesive layer 25 is uniformly applied over one surface of the strip material, as shown in Fig.22.

[0058] A first example of the information carrier manufacturing method according to the present invention is destined for manufacturing the information carrier 20a according to the first exemplary embodiment by using one sheet of strip material 41 shown in Fig. 18 and two sheets of strip materials 45 shown in Fig. 22. At first, one of the strip materials 45 is bonded to one surface of the strip material 41 with the adhesive layer 25 being interposed therebetween to thereby obtain a unitary bonded strip composed of the strip materials 41 and 45 having spaces within which the IC elements 1 can be accommodated, respectively. Subsequently, the IC elements 1 are positioned to be placed within the spaces mentioned above, respectively, whereon the IC elements 1 are bonded to the strip material 45 by using the adhesive layers 25, respectively. In succession, the other strip material 45 is bonded to the other surface of the strip material 41 with the adhesive layer 25 interposed therebetween to thereby realize a unitary bonded strip composed of the strip materials 41 and 45 and having the IC elements 1 accommodated within the internal spaces, respectively. Finally, the unitary bonded strip is cut into segments each of a predetermined shape to obtain the information carriers 20a according to the first embodiment. With the information carrier manufacturing method according to the instant exemplary embodiment, a large number of the IC elements 1 are encased internally of the strip materials 41 and 45 and then the concerned information carriers are formed by punching from the bonded strip materials 41 and 45. Thus, the identical information carriers can be manufactured with high efficiency and hence the manufacturing cost of the information carrier can be reduced.

[0059] A second example of the information carrier manufacturing method according to the present invention is destined for manufacturing the information carrier 20b according to the second exemplary embodiment by using one sheet of the strip material 42 shown in Fig. 19 and two sheets of the strip materials 45 shown in Fig. 22. At first, the booster coils 28 are placed within ring-like recesses 29 formed in the strip material 42 and then the booster coil 28 are bonded to the bottom surfaces of the recesses 29 by using adhesive layers 32, respectively. Subsequently, the strip material 45 is bonded to one of the surfaces of the strip material 42 by using the adhesive layer 25 interposed therebetween to thereby obtain a unitary bonded strip composed of the strip materials 42 and 45 bonded together and having spaces within which the IC elements 1 can be accommodated, respectively. In succession, the IC elements 1 are positioned to be placed within the above-mentioned spaces and bonded to the strip material 45 with the adhesive layer 25. Thereafter, the other sheet of strip material 45 is bonded to the other surface of the strip material 41 with the adhesive layer 25 interposed therebetween to thereby obtain the bonded strip constituted by the strip materials 42 and 45 and having the IC elements 1 accommodated within the internal spaces, respectively. Next, the space within which the IC element 1 has been accommodated is filled with a potting resin 31 to obtain the unitary bonded strip composed of the strip materials 41 and 45 and having the IC elements 1 fixedly embedded therein. Finally, the unitary bonded strip is cut into segments each of a predetermined shape to obtain the information carriers 20e according to the fifth exemplary embodiment. The instant example of the information carrier manufacturing method presents similar advanta-

geous effects as those of the information carrier manufacturing method according to the first embodiment.

[0060] A third example of the information carrier manufacturing method according to the present invention is destined for manufacturing the information carrier 20c according to the third exemplary embodiment by using a single sheet of the strip material 43 shown in Fig. 20 and a single sheet of the strip material 45 shown in Fig. 22. At first, the IC elements 1 are positioned to be placed within the recesses 30, respectively, which are formed in the strip material 43 and then the IC elements are bonded to the bottom surfaces of the recesses 30 by using the adhesive layers 32, respectively. Subsequently, the strip material 45 is bonded to the surface of the strip material 43 formed with the recesses by using the adhesive layer 25 interposed therebetween to thereby obtain a unitary bonded strip which is composed of the strip materials 43 and 45 bonded together and having the IC elements 1 embedded therein. Finally, the unitary bonded strip is cut into segments each of a predetermined shape to thereby obtain the information carriers 20c according to the third exemplary embodiment. The instant example of the information carrier manufacturing method presents similar advantageous effects as those of the information carrier manufacturing method according to the first embodiment.

[0061] A fourth example of the information carrier manufacturing method according to the present invention is destined for manufacturing the information carrier 20d according to the fourth exemplary embodiment by using a single sheet of the strip material 44 shown in Fig. 21 and a single sheet of the strip material 45 shown in Fig. 22. At first, the IC elements 1 are positioned to be placed within the first recesses 30, respectively, which are formed in the strip material 44, and then the IC elements are bonded to the bottom surfaces of the above-mentioned recesses 30 by using the adhesive layers 32, respectively, while the booster coils 28 are accommodated within the second ring-like recesses 29, respectively, which are formed in the strip material 44 and bonded to the bottom surfaces of the above-mentioned recesses 29, respectively, by using the adhesive layers 32 interposed therebetween. Subsequently, the strip material 45 is bonded to the surface of the strip material 44 having the recesses by using the adhesive layer 25 interposed therebetween to thereby obtain a unitary bonded strip which is composed of the strip materials 44 and 45 bonded together and having internal spaces within which the IC elements 1 have been accommodated, respectively. Finally, the unitary bonded strip is cut into segments each of a predetermined shape to obtain the information carriers 20c according to the third exemplary embodiment. The instant example of the information carrier manufacturing method presents similar advantageous effects as those of the information carrier manufacturing method according to the first embodiment.

[0062] A fifth example of the information carrier manufacturing method according to the present invention is destined for manufacturing the information carrier 20e according to the fifth exemplary embodiment by using a single strip material 41 shown in Fig. 18 and a single sheet of strip material 45 shown in Fig. 22. At first, the strip material 45 is bonded to one surface of the strip material 41 with the adhesive layer 25 being interposed therebetween to thereby obtain a bonded strip composed of the strip materials 41 and 45 and having the spaces within which the IC elements 1 can be accommodated, respectively. Subsequently, the IC elements 1 are positioned to be placed within the above-mentioned spaces, respectively, whereon the IC elements are bonded to the strip material 45 by using the adhesive layer 25 interposed therebetween. In succession, the spaces in which the above-mentioned IC elements 1 are accommodated, respectively, are each filled with the potting resin 31 to thereby obtain the unitary bonded strip constituted by the strip materials 41 and 45 and having the IC elements 1 embedded therein. Finally, the unitary bonded strip is cut into segments each of a predetermined shape to obtain the information carriers 20e according to the fifth exemplary embodiment. The instant example of the information carrier manufacturing method equally presents similar advantageous effects as those of the information carrier manufacturing method according to the first embodiment.

[0063] A sixth example of the information carrier manufacturing method according to the present invention is destined for manufacturing the information carrier 20f according to the sixth exemplary embodiment by using one sheet of the strip material 42 shown in Fig. 19 and a single sheet of the strip material 45 shown in Fig. 22. At first, the booster coils 28 are placed within the ring-like recesses 29, respectively, which are formed in the strip material 42, and then the booster coils 28 are bonded to the bottom surfaces of the recesses 29 by using the adhesive layers 32, respectively. Subsequently, the strip material 45 is bonded to one of the surfaces of the strip material 42 by using the adhesive layer 25 interposed therebetween to thereby obtain a bonded strip composed of the strip materials 42 and 45 bonded together and having the spaces within which the IC elements 1 can be accommodated, respectively. In succession, the IC elements 1 are positioned to be placed within the above-mentioned spaces, respectively, and bonded to the strip material 45 with the adhesive layer 25 interposed therebetween. In succession, the recesses 29 in which the above-mentioned booster coils 28 are accommodated and the spaces in which the above-mentioned IC elements 1 are accommodated are each filled with the potting resin 31 to thereby obtain the unitary bonded strip constituted by the strip materials 42 and 45 and having the IC elements 1 and the booster coils 28 which are embedded therein. Finally, the unitary bonded strip is cut into segments each of a predetermined shape to obtain the information carriers 20f according to the sixth exemplary embodiment. The instant

example of the information carrier manufacturing method equally presents similar advantageous effects as those of the information carrier manufacturing method according to the first embodiment.

[0064] A seventh example of the information carrier manufacturing method according to the present invention is destined for manufacturing the information carrier 20g according to the seventh exemplary embodiment by using a single sheet of the strip material 43 shown in Fig. 20. At first, the IC elements 1 are positioned to be accommodated within recesses 30, respectively, which are formed in the strip material 43 and then the IC elements are bonded to the bottom surfaces of the recesses 30, respectively, by using the adhesive layers 32, respectively. In succession, the recesses 30 in which the above-mentioned IC elements 1 are accommodated are each filled with the potting resin 31 to thereby obtain the strip material 43 having the IC elements 1 embedded therein. Finally, this strip material 43 is cut into segments each of a predetermined shape to obtain the information carriers 20g according to the seventh exemplary embodiment. The instant example of the information carrier manufacturing method equally presents similar advantageous effects as those of the information carrier manufacturing method according to the first embodiment.

[0065] An eighth example of the information carrier manufacturing method according to the present invention is destined for manufacturing the information carrier 20h according to the eighth exemplary embodiment by using a single sheet of the strip material 44 shown in Fig. 21. At first, the IC elements 1 are positioned to be accommodated within the first recesses 30, respectively, which are formed in the strip material 43 and then the IC elements are bonded to the bottom surfaces of the recesses 30, respectively, by using the adhesive layers 32, respectively, while the booster coils 28 are accommodated within the second ring-like recesses 29, respectively, which are formed in the strip material 44 and then the booster coils are bonded to the bottom surfaces of the recesses 29 by using the adhesive layers 32, respectively. In succession, the first recesses 30 in which the above-mentioned IC elements 1 are accommodated and the second recesses 29 in which the above-mentioned booster coils 28 are accommodated are each filled with the potting resin 31 to thereby obtain the strip material 43 having the IC elements 1 and the booster coils 28 embedded therein. Finally, this strip is cut into segments each of a predetermined shape to obtain the information carriers 20h according to the eighth exemplary embodiment. The instant example of the information carrier manufacturing method equally presents similar advantageous effects as those of the information carrier manufacturing method according to the first embodiment.

[0066] Incidentally, in the second, fourth, sixth and eighth exemplary embodiments described above, the booster coil 28 is formed separately or independently from the substrate 21, the booster coil 28 may be formed by printing on any one of the strip materials constituting the substrate 21.

[0067] As is apparent from the foregoing description, in the IC element according to the present invention, the electric conductor of the coil formed integrally with the IC element is implemented in a multilayer structure including the metal-sputtered layer or alternatively metal-evaporated layer and the metal-plated layer. Thus, when compared with the IC element in which the electric conductor is formed only of the metal-sputtered layer or alternatively metal-evaporated layer, loss of the electromagnetic energy can be reduced, which can contribute to stabilization of electric power reception from the reader/writer, stabilization of communication with the reader/writer and extension of the communication range relative to the reader/writer.

[0068] In the IC element manufacturing method according to the present invention, a large number of coils corresponding to the individual IC elements, respectively, can simultaneously be formed in the finished wafer instead of forming the coil in each of the IC elements. Thus, the IC element formed internally with the coil can be manufactured with high efficiency, as a result of which this sort of IC element can be manufactured at low cost.

[0069] In the information carrier according to the present invention, the IC element formed integrally with the coil is disposed at a center portion of the substrate as viewed in the planar direction, i.e., perpendicularly to the plane of the substrate. Thus, the center of the coil formed integrally with the IC element and that of the antenna coil of the reader/writer can easily be aligned with each other, which means that the electromagnetic coupling coefficient between both the coils is increased, whereby the electric power supply to the information carrier from the reader/writer as well as the signal transmission/reception between the reader/writer and the information carrier can be stabilized.

[0070] In the information carrier manufacturing method according to the present invention, the unitary strip in which the required parts to be mounted inclusive of the IC elements are mounted on the strip material is manufactured, whereon the concerned information carriers are formed by punching the unitary strip. Thus, the identical information carriers can be manufactured with high efficiency, whereby the cost involved in manufacturing the information carriers each incorporating the IC element can be reduced.

[0071] According to further aspects of the present invention, the following may be provided:

[0072] An IC element formed integrally with a coil for performing contactless data communication with external equipment, characterized in that a conductor constituting said coil is implemented in a multilayer structure including: a metal-sputtered layer or alternatively a metal-evaporated layer; and a metal-plated layer.

[0073] Advantageously, said metal-sputtered layer, or alternatively said metal-evaporated layer, is formed of

at least one metal of aluminum, nickel, copper and chromium or alternatively an alloy containing those metals, and

said metal-plated layer deposited on said metal-sputtered layer, or alternatively said metal-evaporated layer, is formed of copper.

[0074] Advantageously, said coil is formed on a surface of said IC element formed with input/output terminals with interposition of an electrically insulative surface passivation film, and

the input/output terminals of said IC element and said coil are electrically interconnected through through-holes formed in said surface passivation film, each through-hole having a diameter smaller than a line width of said coil.

[0075] Advantageously, said coil is implemented in a rectangular spiral pattern in a planar shape and all or some of comer portions of said rectangular spiral pattern are chamfered.

[0076] Advantageously, said metal-plated layer is formed by an electroless plating method, or alternatively an electroplating method, or alternatively a precision electroforming method.

[0077] Advantageously, a line width of said coil is not smaller than 7 μm, an inter-line distance thereof is not greater than 5μm and the number of turns thereof is not smaller than 20 turns.

[0078] A method of manufacturing an IC element, wherein said method comprises:

forming uniformly a metal-sputtered layer, or alternatively a metal-evaporated layer, on a surface passivation film of a finished wafer manufactured through a predetermined process;

forming uniformly a photoresist layer on said metal-sputtered layer, or alternatively said metal-evaporated layer;

forming in said photoresist layer a predetermined pattern inclusive of a coil for contactless data communication with external equipment through light exposure and development to thereby expose said metal-sputtered layer, or alternatively said metal-evaporated layer, through said predetermined pattern;

laminating a metal-plated layer on exposed portions of said metal-sputtered layer, or alternatively said metal-evaporated layer, through an electroless plating method, or alternatively an electroplating method, or alternatively a precision electroforming method,

eliminating the photoresist layer deposited on said finished wafer;

forming a predetermined conductor pattern corresponding to said predetermined pattern by etching said metal-sputtered layer, or alternatively said metal-evaporated layer, exposed through said metal-plated layer;

obtaining concerned IC elements each formed integrally with a coil by scribing said finished wafer.

[0079] A method of manufacturing an IC element, characterized in that said method comprises a step of forming uniformly a photoresist layer on a surface passivation film of a finished wafer manufactured through a predetermined process, a step of forming in said photoresist layer a predetermined pattern inclusive of a coil for contactless data communication with external equipment through light exposure and development to thereby expose said surface passivation film in said predetermined pattern, a step of mounting the finished wafer undergone a development processing on a sputtering apparatus or alternatively a vacuum evaporation apparatus and forming a metal-sputtered layer or alternatively a metal-evaporated layer on exposed portions of said surface protection film, a step of eliminating the photoresist layer deposited on said finished wafer, a step of forming a metal-plated layer on said metal-sputtered layer or alternatively on said metal-evaporated layer by resorting to an electroless plating method or alternatively an electroplating method, and a step of obtaining concerned IC elements each formed integrally with a coil by scribing said finished wafer.

[0080] An information carrier including a substrate having mounted thereon an IC element formed integrally with an antenna coil for performing data communication in a contactless manner with external equipment, wherein said IC element is disposed at a center portion of said substrate in a planar direction perpendicularly to a plane of said substrate.

[0081] Advantageously, both of top and bottom surfaces of said IC element are covered by said substrate.

[0082] Advantageously, only one surface of said IC element is covered with said substrate.

[0083] Advantageously, said substrate is formed in a circular or square planar shape.

[0084] Advantageously, said substrate is wholly or partially formed of paper.

[0085] Advantageously, said substrate is implemented in a three-bonded-layer structure including a top member, a bottom member and an intermediate member, and said IC element is accommodated within a through-hole formed in said intermediate member at a mid portion thereof.

[0086] Advantageously, said through-hole is formed circularly in a planar shape.

[0087] Advantageously, said substrate is implemented in a two-bonded-layer structure including a top member and a bottom member, and said IC element is accommodated within a recess formed in said top member, or alternatively in said bottom member at a mid portion thereof.

[0088] Advantageously, said substrate is implemented in a single layer structure and said IC element is accommodated within a recess formed in said substrate at a mid portion thereof.

[0089] Advantageously, said recess is formed circu-

larly in a plane shape.

[0090] Advantageously, the information carrier further comprises another discrete coil which is separately formed independent of said IC element internally of said substrate.

[0091] An information carrier manufacturing method comprising:

bonding together a first strip material having regularly formed therein a number of through-holes in which IC elements can be inserted, respectively, and a second stri material formed with no through-hole,
placing and fixing the IC elements each formed integrally with a coil in said through-holes, respectively,
bonding together said first strip material and a third strip material provided with no through-hole,
punching said first to third strip materials bonded unitarily to thereby obtain the concerned information carriers each incorporating said IC element.

[0092] An information carrier manufacturing method, comprising:

placing and fixing coils formed separately independent of IC elements in a number of ring-like recesses formed in a first strip material concentrically around through-holes, respectively, which are formed regularly in said first strip material and capable of accommodating said IC elements, respectively,
bonding a second strip material having no through-hole onto one surface of said first strip material,
placing fixedly said IC elements each formed integrally with a coil in siad through-holes, respectively,
bonding together said first strip material and a third strip material having no through-hole, and
punching said first to third strip materials bonded unitarily to thereby obtain desired information carriers each including the IC element and the coil formed separately independent of said IC element.

[0093] An information carrier manufacturing method, comprising:

placing fixedly IC elements each formed integrally with a coil in a number of recesses for accommodating the IC elements, respectively, which recesses are regularly formed in a first strip material,
bonding a second strip material having no through-hole onto a surface of said first strip material in which no through-holes are formed, and
punching the first and second strip materials bonded unitarily to thereby obtain desired information carriers each incorporating said IC element.

[0094] An information carrier manufacturing method, comprising:

placing fixedly IC elements each formed integrally with a coil in a number of first recesses formed regularly in a first strip material which has second recesses each formed in a ring-like shape concentrically around said first recesses, respectively, said first recesses being capable of accommodating said IC elements, respectively,
placing fixed coils formed discretely independent of said IC elements within said second recesses, respectively, formed in said first strip material,
bonding a second strip material having no through-hole onto a surface of said first strip material in which said recesses are formed, and
punching said first and second strip materials bonded unitarily to thereby obtain desired information carriers each including the IC element and the coil formed discretely independent of said IC element.

[0095] An information carrier manufacturing method, comprising:

bonding together a first strip material having a number of through-holes formed regularly and allowing IC elements to be inserted therein, respectively, and a second strip material having no through-hole,
placing and fixing said IC elements each formed integrally with a coil in said through-holes, respectively,
sealing off said through-holes having said IC elements accommodated therein, and
punching the first and second strip materials bonded unitarily to thereby obtain desired information carriers each incorporating said IC element.

[0096] An information carrier manufacturing method, comprising:

placing and fixing coils formed separately independent of IC elements in a number of ring-like recesses formed in a first strip material concentrically around through-holes, respectively, which are formed regularly in said first strip material and capable of accommodating said IC elements, respectively,
bonding together said first strip material and a second strip material having no through-hole,
sealing off said through-holes having said coils accommodated threin with a resin, and
punching said first and second strip materials bonded unitarily to thereby obtain desired information carriers each including said IC element and the associated coil formed separately independent of said IC element.

[0097] An information carrier manufacturing method,

comprising:

placing fixedly IC elements each formed integrally with a coil in a number of recesses for accommodating said IC elements, respectively, said recesses being regularly formed in a strip material,
sealing off said recesses having said IC elements accommodated therein with a resin, and
punching said strip material to thereby obtain desired information carriers each incorporating said IC element.

[0098] An information carrier manufacturing method, comprising:

placing fixedly IC elements each formed integrally with a coil in a number of first recesses, respectively, which are formed regularly in a strip material having second ring-like recesses formed concentrically around said first recesses, respectively, said first recesses being capable of accommodating said IC elements, respectively,
placing fixedly coils formed discretely independent of said IC elements within said second recesses, respectively, of said strip material,
sealing off said first and second recesses with a resin, and
punching said strip material to thereby obtain desired information carriers each including the IC element and the coil formed discretely independent of said IC element.

Claims

1. A method for manufacturing an IC element in which antenna coil for wireless communication is uniformly formed, said method comprising at least steps of:

   forming a conductive pattern at least including plurality of antenna coil for wireless communication over a surface protection film of a wafer formed by a predetermined process; and
   obtaining an IC element in which a single antenna coil is uniformly formed by way of a scriber wafer on which said conductive pattern is formed.

2. A method for manufacturing an IC element in accordance with claim 1, wherein said step of forming a conductive pattern further comprises at least steps of:

   forming a metal sputtering layer or a metal deposition layer, and
   forming metal plating on said metal sputtering layer or metal deposition layer.

3. A method for forming an IC element in an IC element according to claim 2, wherein said metal plating layer is formed by non-electrolytic plating, electrolytic plating or precision electroforming.

FIG. 1A

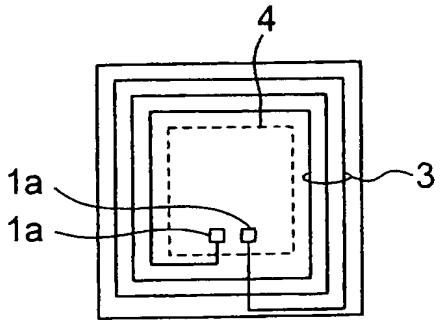


FIG. 1B

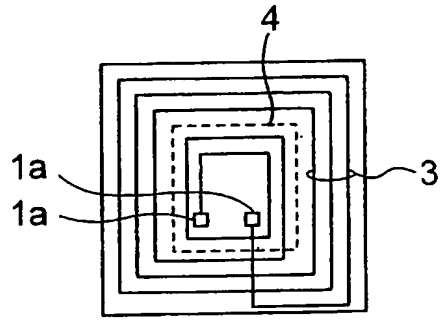


FIG. 1C

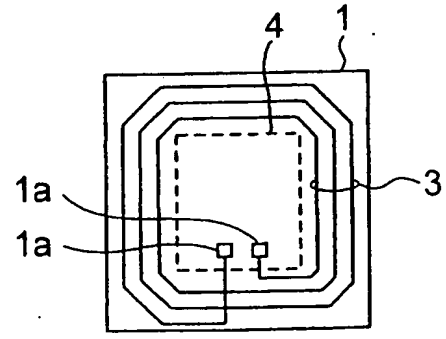


FIG. 2A

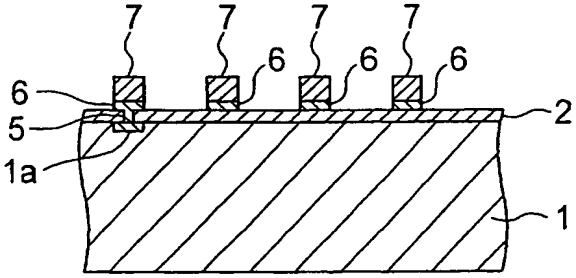


FIG. 2B

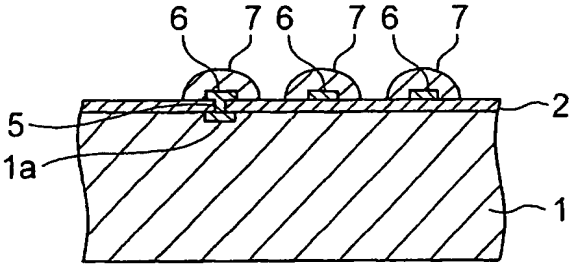


FIG. 3

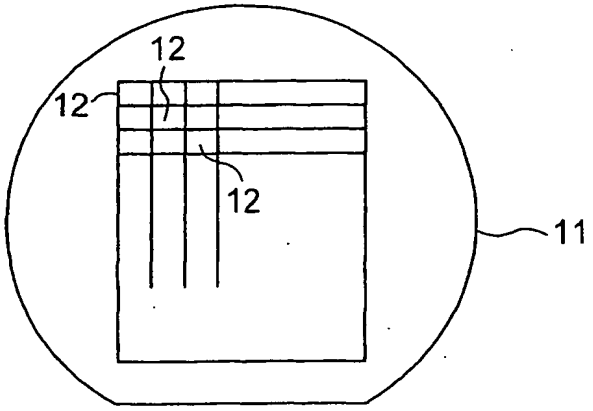


FIG. 4A

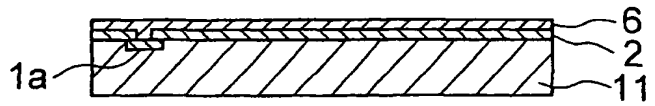


FIG. 4B

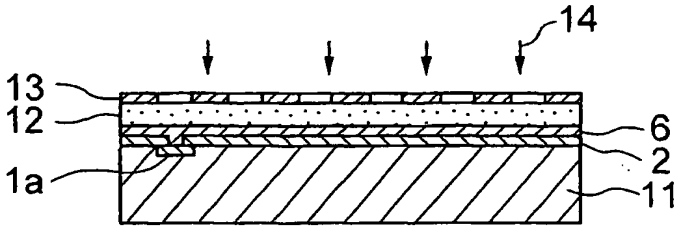


FIG. 4C

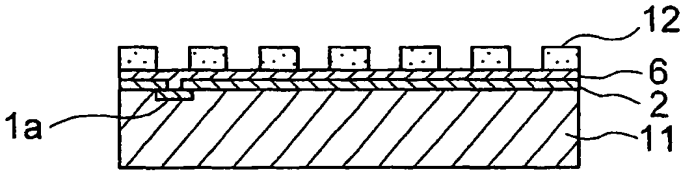


FIG. 4D

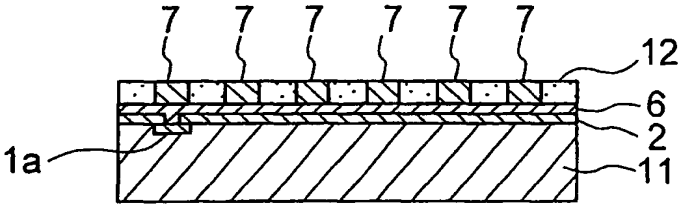


FIG. 4E

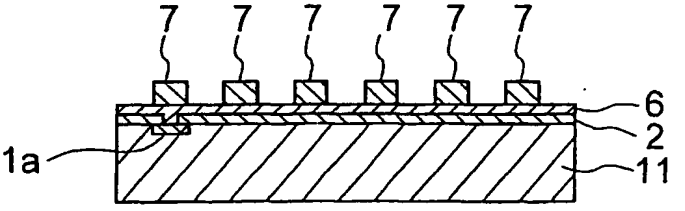


FIG. 4F

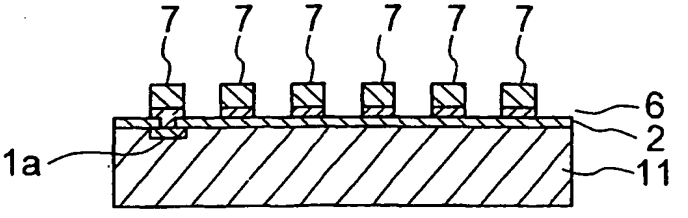


FIG. 5A

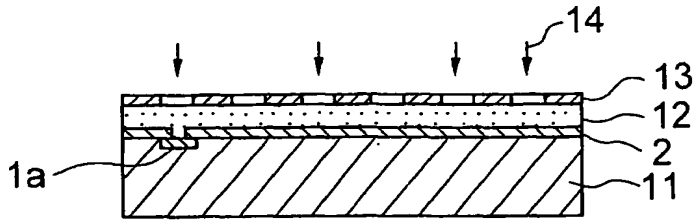


FIG. 5B

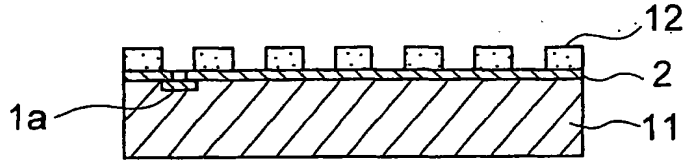


FIG. 5C

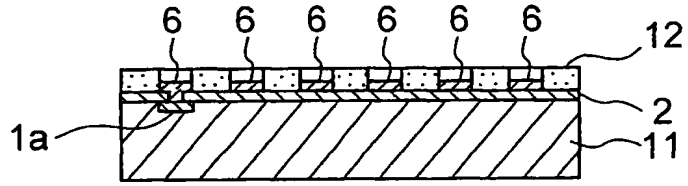


FIG. 5D

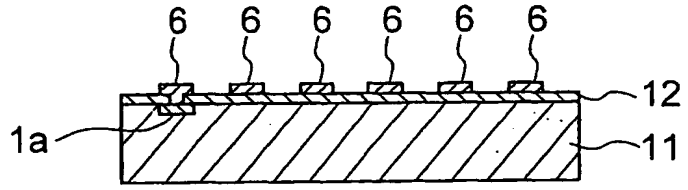


FIG. 5E

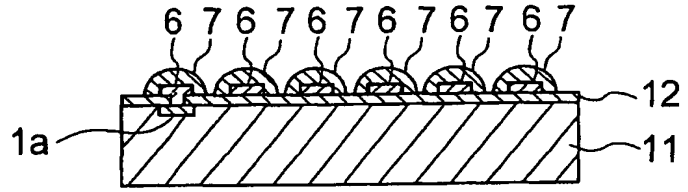


FIG. 6

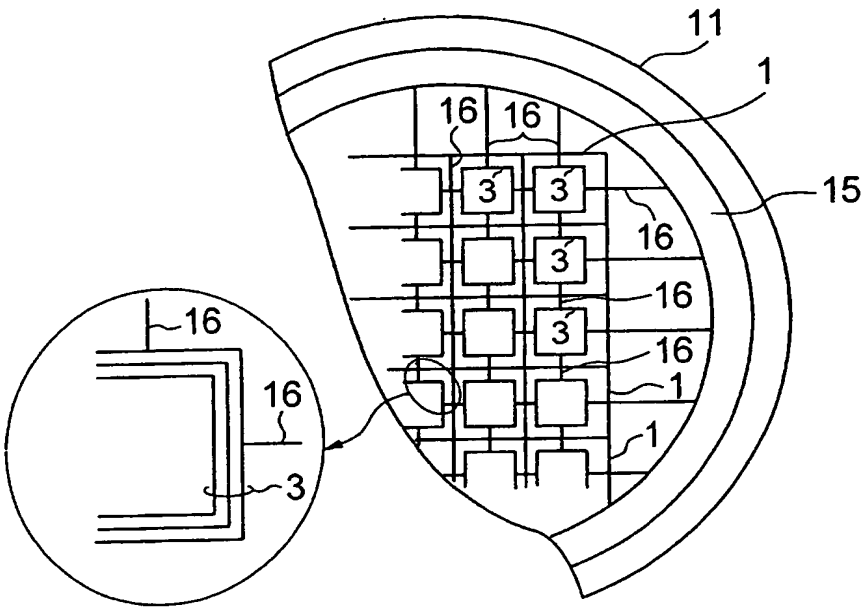


FIG. 7

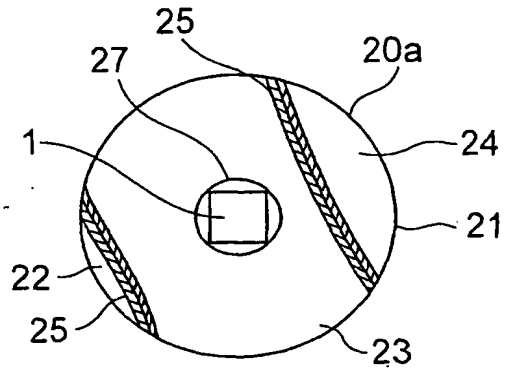


FIG. 8

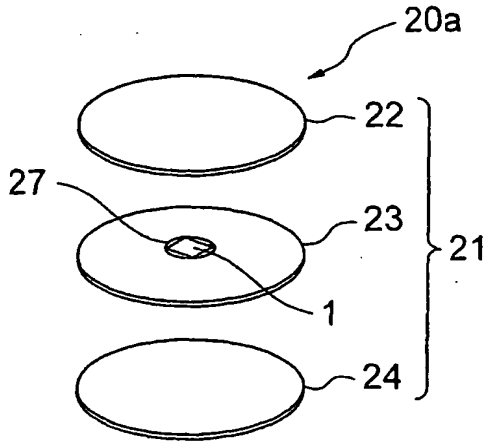


FIG. 9

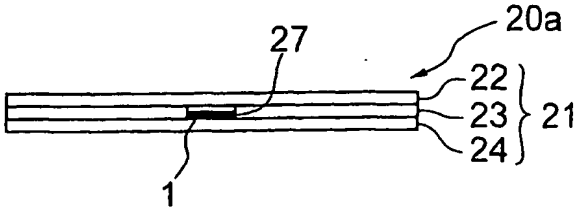


FIG. 10

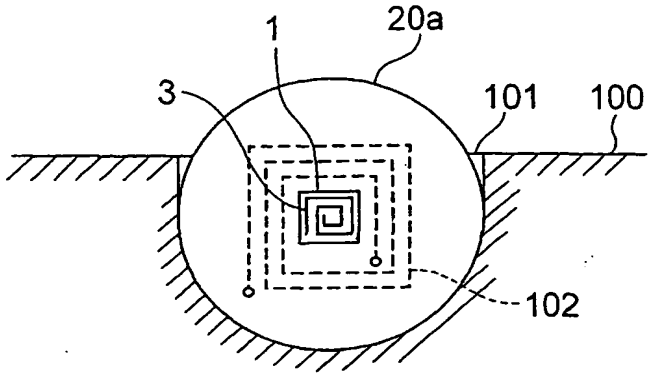


FIG. 11

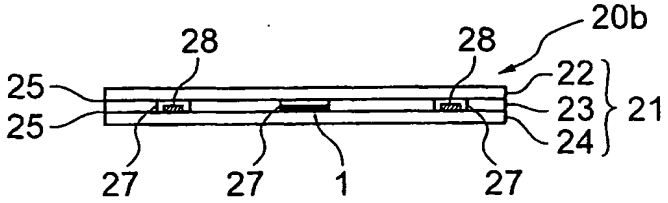


FIG. 12

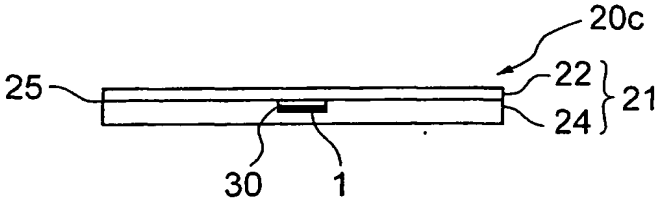


FIG. 13

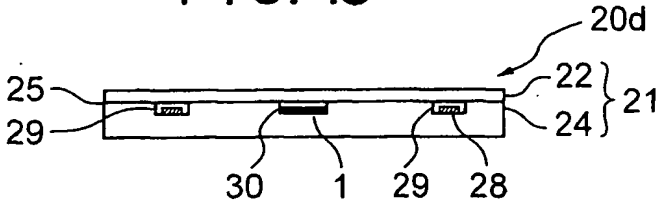


FIG. 14

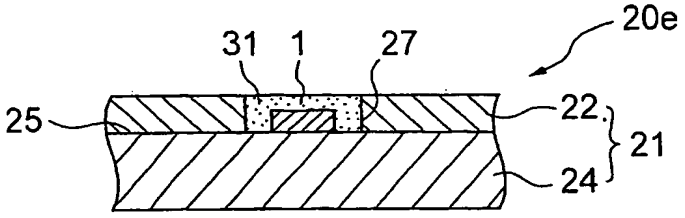


FIG. 15

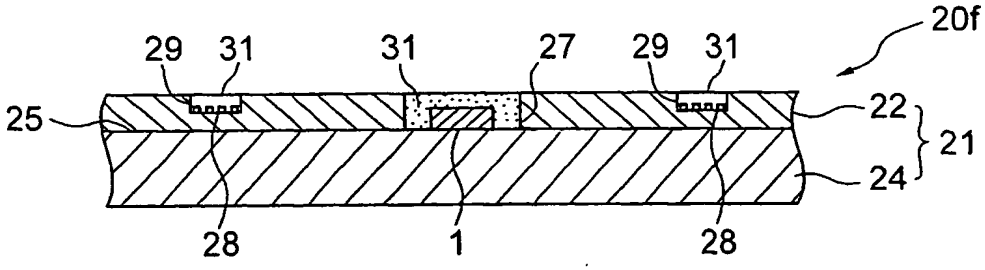


FIG. 16

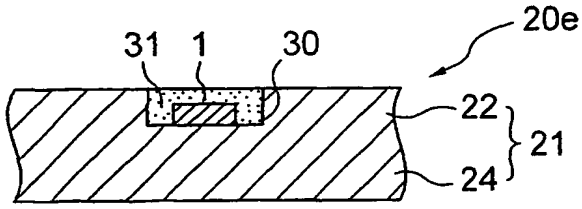


FIG. 17

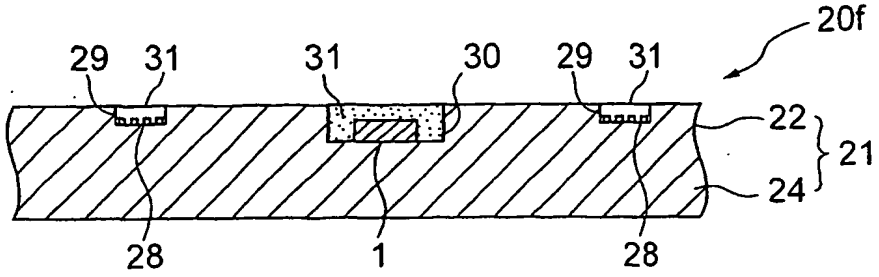


FIG. 18

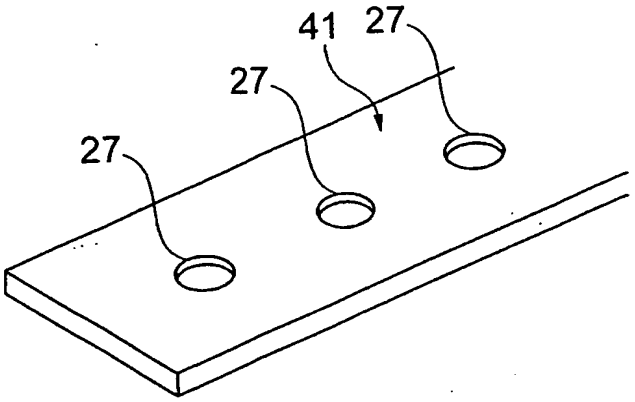


FIG. 19

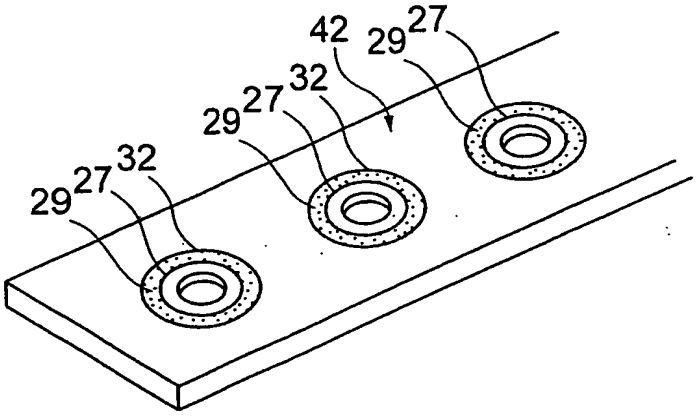


FIG. 20

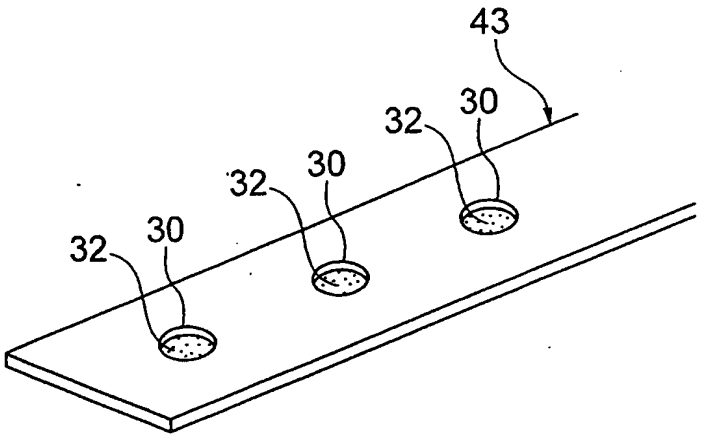


FIG. 21

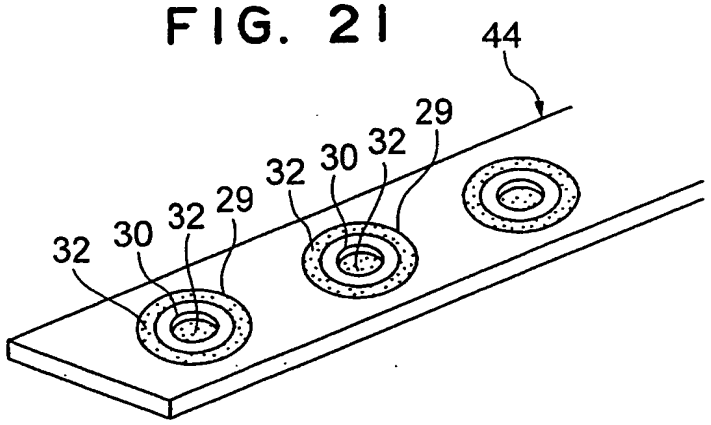
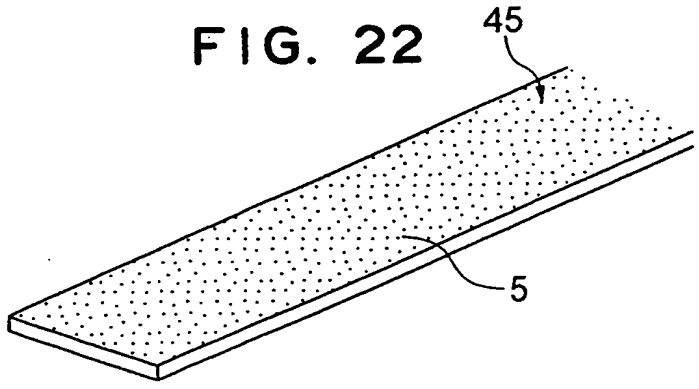


FIG. 22



European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 04 01 3387

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	WO 92/08209 A (JURISCH REINHARD) 14 May 1992 (1992-05-14) * page 3, line 10 - page 3, line 32 *	1-3	G06K19/07 H01L23/50
A	PATENT ABSTRACTS OF JAPAN vol. 1996, no. 12, 26 December 1996 (1996-12-26) & JP 8 222695 A (HITACHI LTD), 30 August 1996 (1996-08-30) * abstract *	1-3	
A	PATENT ABSTRACTS OF JAPAN vol. 0102, no. 72 (E-437), 16 September 1986 (1986-09-16) & JP 61 094339 A (ROHM CO LTD), 13 May 1986 (1986-05-13) * abstract *	1-3	
A	PATENT ABSTRACTS OF JAPAN vol. 0101, no. 64 (E-410), 11 June 1986 (1986-06-11) & JP 61 016591 A (ROOMU KK), 24 January 1986 (1986-01-24) * abstract *	1-3	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

G06K
H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	16 July 2004	Gronau von, H-C

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 04 01 3387

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

16-07-2004

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9208209 A	14-05-1992	DE 4034225 A1	30-04-1992
		AT 153790 T	15-06-1997
		WO 9208209 A1	14-05-1992
		EP 0507903 A1	14-10-1992
		US 5308967 A	03-05-1994
JP 8222695 A	30-08-1996	NONE	
JP 61094339 A	13-05-1986	NONE	
JP 61016591 A	24-01-1986	NONE	

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 00000PCT7721	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/JP2005/001541	International filing date *(day/month/year)* 27.01.2005	(Earliest) Priority Date *(day/month/year)* 06.02.2004
Applicant SEMICONDUCTOR ENERGY LABORATORY CO., LTD.		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

☐ the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

b. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (See Box II).

3. ☐ **Unity of invention is lacking** (See Box III).

4. With regard to the **title**,

☑ the text is approved as submitted by the applicant.

☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

☑ the text is approved as submitted by the applicant.

☐ the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the drawings,

a. the figure of the drawings to be published with the abstract is Figure No. 1A

☑ as suggested by the applicant.

☐ as selected by this Authority, because the applicant failed to suggest a figure.

☐ as selected by this Authority, because this figure better characterizes the invention.

b. ☐ none of the figures is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2005/001541

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl⁷ H01L 27/12, H01L 29/786, H01L 21/336, G06K 19/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl⁷ H01L 27/12, H01L 29/786, H01L 21/336, G06K 19/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Japanese Utility Model Gazette 1922-1996, Japanese Publication of Unexamined Utility Model Applications 1971-2005, Japanese Registered Utility Model Gazette 1994-2005, Japanese Gazette Containing the Utility Model 1996-2005

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2001/0015256 A1 (Semiconductor Energy Laboratory) 2001.08.23,whole document, Figs.1-9C &JP 2001-272923 A	1-60
Y	WO 2003/010825 A1(SEIKO EPSON CORPORATION) 2003.02.06,whole document, Figs.1-34 (Family:none)	1-60
Y	EP 1193759 A(HITACHI MAXELL, LTD.) 2002.04.03,whole document, Figs.1-22 &WO 2000/051181 A1 &JP 2002-343877 A	23-25

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
03.03.2005	22.3.2005
Name and mailing address of the ISA/JP **Japan Patent Office** 3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan	Authorized officer Sonoko Miyazaki 4M 3123 Telephone No. +81-3-3581-1101 Ext. 3462

Form PCT/ISA/210 (second sheet) (January 2004)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
SEMICONDUCTOR ENERGY
LABORATORY CO., LTD.

398, Hase, Atsugi-shi,
Kanagawa
2430036
Japan

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	22. 3. 2005
Applicant's or agent's file reference: 00000PCT7721	FOR FURTHER ACTION: See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/JP2005/001541	27.01.2005	06.02.2004

International Patent Classification (IPC) or both national classification and IPC
Int.Cl⁷ H01L 27/12, H01L 29/786, H01L 21/336, G06K 19/00

Applicant
SEMICONDUCTOR ENERGY LABORATORY CO., LTD.

1. This opinion contains indications relating to the following items:

- [x] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [x] Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. FURTHER ACTION

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Date of completion of this opinion: 03.03.2005	
Name and mailing address of the ISA/JP **Japan Patent Office** 3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan	Authorized officer: Sonoko Miyazaki (4M 3123) Telephone No. +81-3-3581-1101 Ext. 3462

Form PCT/ISA/237 (cover sheet) (January 2004)

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/JP2005/001541

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   ☐ This opinion has been established on the basis of a translation from the original language into the following language _____, which is the language of a translation furnished for the purposes of international search (under Rules 12.3 and 23.1(b)).

2. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:

   a. type of material

   ☐ a sequence listing
   ☐ table(s) related to the sequence listing

   b. format of material

   ☐ in written format
   ☐ in computer readable form

   c. time of filing/furnishing

   ☐ contained in the international application as filed.
   ☐ filed together with the international application in computer readable form.
   ☐ furnished subsequently to this Authority for the purposes of search.

3. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

4. Additional comments:

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/JP2005/001541

Box No. V **Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	1-60	YES
	Claims		NO
Inventive step (IS)	Claims		YES
	Claims	1-60	NO
Industrial applicability (IA)	Claims	1-60	YES
	Claims		NO

2. Citations and explanations

D1:US 2001/0015256 A1(Semiconductor Energy Laboratory)
2001.08.23,whole document, Figs.1-9C
D2:WO 2003/010825 A1(SEIKO EPSON CORPORATION)
2003.02.06,whole document, Figs.1-34
D3:EP 1193759 A(HITACHI MAXELL, LTD.)
2002.04.03,whole document, Figs.1-22

[Claims 1-3]
The subject matter of claims 1-3 does not appear to involve an inventive step in view of the cited documents D1- D2.
D1 discloses a method for manufacturing a thin film integrated circuit, comprising the steps of: forming a separation layer over an insulating substrate; forming at least two thin film integrated circuits over the separation layer; forming a groove between the two thin film integrated circuits to expose the separation layer; separating the insulating substrate by introducing etchant into the groove and removing the separation layer.
D2 discloses the thin film integrated circuits are imprinted to a wireless IC tag.

[Claims 4-7]
The subject matter of claims 4-7 does not appear to involve an inventive step in view of the cited documents D1- D2.
D1 discloses attaching the two thin film integrated circuits to a flexible substrate.

[Claims 8-10]
The subject matter of claims 8-10 does not appear to involve an inventive step in view of the cited documents D1- D2.
D1 discloses the nitrogen oxide film is over the thin film integrated circuits.

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

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Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of: Box No.V

[Claims 11-13]
The subject matter of claims 11-13 does not appear to involve an inventive step in view of the cited documents D1- D2.
D1 discloses separating the insulating substrate by introducing etchant into the groove and removing the separation layer and the etchant gas including halide typified by ClF3.

[Claims 14-16]
The subject matter of claims 14-16 does not appear to involve an inventive step in view of the cited documents D1- D2.
D1 discloses the insulating substrate is a glass substrate or a quartz substrate.

[Claims 17-19]
The subject matter of claims 17-19 does not appear to involve an inventive step in view of the cited documents D1- D2.
A mounting position of each of the two thin film integrated circuits is a matter of design.

[Claims 20-22]
The subject matter of claims 20-22 does not appear to involve an inventive step in view of the cited documents D1- D2.
D1 discloses two substrates are attached by an ultrasonic adhesive.

[Claims 23-25]
The subject matter of claims 23-25 does not appear to involve an inventive step in view of the cited documents D1- D3.
D3 discloses the antenna is formed by sputtering method or plating method.

[Claims 26-28]
The subject matter of claims 26-28 does not appear to involve an inventive step in view of the cited documents D1- D2.
D1 discloses that the separate layer is an amorphous semiconductor.

[Claims 29-40]
The subject matter of claims 29-40 does not appear to involve an inventive step in view of the cited documents D1- D2.
The thickness of two thin film integrated circuits and the semiconductor film is a matter of design.
A hydrogen concentration of semiconductor film is a matter of design.

[Claims 41-43]
The subject matter of claims 41-43 does not appear to involve an inventive step in view of the cited documents D1- D2.
The arrangement direction of a thin film transistor to a mount article is a matter of design.

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Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of: Box No.V

[Claims 44-46]
The subject matter of claims 41-43 does not appear to involve an inventive step in view of the cited documents D1- D2.
D2 discloses that the groove is formed by dicing.

[Claims 47-48]
The subject matter of claims 47-48 does not appear to involve an inventive step in view of the cited documents D1- D2.
D1 discloses an element substrate comprising: an insulating substrate; a separation layer over the insulating layer; at least two thin film integrated circuits over the separation layer; and a groove provided between the two thin film integrated circuits.
D2 discloses the thin film integrated circuits are imprinted to a wireless IC tag.

[Claims 49-50]
The subject matter of claims 49-50 does not appear to involve an inventive step in view of the cited documents D1- D2.
D1 discloses the nitrogen oxide film is over the thin film integrated circuits.

[Claims 51-52]
The subject matter of claims 51-52 does not appear to involve an inventive step in view of the cited documents D1- D2.
D1 discloses that the separate layer is an amorphous semiconductor.

[Claims 53-58]
The subject matter of claims 53-58 does not appear to involve an inventive step in view of the cited documents D1- D2.
The thickness of two thin film integrated circuits and the semiconductor film is a matter of design.
A hydrogen concentration of semiconductor film is a matter of design.

[Claims 59-60]
The subject matter of claims 59-60 does not appear to involve an inventive step in view of the cited documents D1- D2.
D2 discloses the element substrate is mounted with a banknote or a card.

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

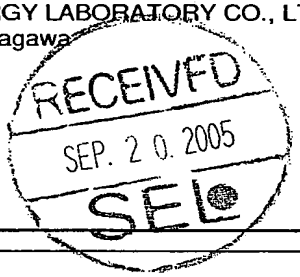
PCT

FIRST NOTICE INFORMING THE APPLICANT OF THE COMMUNICATION OF THE INTERNATIONAL APPLICATION (TO DESIGNATED OFFICES WHICH DO NOT APPLY THE 30 MONTH TIME LIMIT UNDER ARTICLE 22(1))

(PCT Rule 47.1(c))

To:

SEMICONDUCTOR ENERGY LABORATORY CO., LTD.
398, Hase, Atsugi-shi, Kanagawa
2430036
JAPON



Date of mailing *(day/month/year)* 09 September 2005 (09.09.2005)	
Applicant's or agent's file reference 00000PCT7721 WO 8203	**IMPORTANT NOTICE**

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/JP2005/001541	27 January 2005 (27.01.2005)	06 February 2004 (06.02.2004)

Applicant
SEMICONDUCTOR ENERGY LABORATORY CO., LTD. et al

1. **ATTENTION**: For any designated Office(s), for which the time limit under Article 22(1), as in force from 1 April 2002 (30 months from the priority date), **does apply**, please see Form PCT/IB/308(Second and Supplementary Notice) (to be issued promptly after the expiration of 28 months from the priority date).

2. Notice is hereby given that the following designated Office(s), for which the time limit under Article 22(1), as in force from 1 April 2002, **does not apply**, has/have requested that the communication of the international application, as provided for in Article 20, be effected under Rule 93*bis*.1. The International Bureau has effected that communication on the date indicated below:
18 August 2005 (18.08.2005)

   CH

   In accordance with Rule 47.1(c-*bis*)(i), those Offices will accept the present notice as conclusive evidence that the communication of the international application has duly taken place on the date of mailing indicated above and no copy of the international application is required to be furnished by the applicant to the designated Office(s).

3. The following designated Offices, for which the time limit under Article 22(1), as in force from 1 April 2002, **does not apply**, have not requested, as at the time of mailing of the present notice, that the communication of the international application be effected under Rule 93*bis*.1 :

   LU, SE, TZ, UG, ZM

   In accordance with Rule 47.1(c-*bis*)(ii), those Offices accept the present notice as conclusive evidence that the Contracting State for which that Office acts as a designated Office does not require the furnishing, under Article 22, by the applicant of a copy of the international application.

4. **TIME LIMITS for entry into the national phase**

   For the designated Office(s) listed above, and unless a demand for international preliminary examination has been filed before the expiration of **19 months** from the priority date (see Article 39(1)), the applicable time limit for entering the national phase will, **subject to what is said in the following paragraph,** be **20 MONTHS** from the priority date.

   In practice, **time limits other than the 20-month time limit** will continue to apply, for various periods of time, in respect of certain of the designated Offices listed above. For **regular updates on the applicable time limits** (20 or 21 months, or other time limit), Office by Office, refer to the *PCT Gazette*, the *PCT Newsletter* and the *PCT Applicant's Guide*, Volume II, National Chapters, all available from WIPO's Internet site, at http://www.wipo.int/pct/en/index.html.

   It is the applicant's **sole responsibility** to monitor all these time limits.

The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland	Authorized officer Yoshiko Kuwahara
Facsimile No.+41 22 740 14 35	Facsimile No.+41 22 338 90 90